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EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,468	LOWREY ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *78-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *78-99* is/are rejected.

7)☒ Claim(s) *100* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicant's arguments and the amendment to the claims, the rejections of claims 78, 93, 95, and 97, under 35 U.S.C. 112 second paragraph, as being indefinite, are withdrawn.

In view of Applicant's arguments and the amendment to the claims, the objections of claims 80 and 93 are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 88-97 are rejected under 35 U.S.C. 102 (a) or (e) as being anticipated by Prall et al. (U:S. Patent No. 5,866,453)

In re claim 88, Prall et al. disclose the method of manufacturing a semiconductor device having capacitors thereon, comprising the steps of:

forming first and second capacitor (42, see Figure 8A or 18) electrodes supported by a semiconductor substrate, each said capacitor electrode having a portion extending vertically relative to said substrate, said first and second capacitor electrodes being electrically isolated from each other;

forming a first dielectric layer (44) extending over at least a portion of both of said first and second capacitor electrodes, said first dielectric layer extending over at least an uppermost portion of each of said first and second electrodes (see Figure 8A and 18)

forming a conductive layer (46) extending over said first dielectric layer and above said first and second capacitor electrodes;

selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (bottom/side portion of horizontal portion of 44, see Figure 8A), and to expose second and third portions of said first dielectric layer relatively remote from said substrate (top portion of horizontal portion of 44 exposed, and portion of vertical portion of 44 exposed see Figure 8A), and to electrically isolate sections of said conductive layer to form a third capacitor electrode (rightmost 46) in contact with a portion of said first dielectric layer proximate said first capacitor electrode, and a fourth capacitor electrode (leftmost 46) in contact with a portion of said first dielectric layer proximate said second capacitor electrode, said third and fourth capacitor electrodes forming cell electrodes of respective first and second capacitors and being electrically isolated from one another; and

forming a second dielectric layer (56) over said exposed portions of said first dielectric layer and over said third and fourth capacitor electrodes.

The examiner notes that Prall et al. disclose selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (bottom/side portion of horizontal portion of 44, see Figure 8A), and to expose second and third portions of said first dielectric layer relatively remote from said substrate (top portion of horizontal portion of 44 exposed, and portion of vertical portion of 44 exposed see Figure 8A). Furthermore, the examiner notes that the terms relatively remote and relatively proximate are broad. The examiner reads these terms to require one portion to be closer to the substrate and one portion to be further from the substrate.

In re claim 89, Prall et al. disclose the method further comprising the step of forming a conductive line (60) extending through said second dielectric layer (56) and contacting said third and fourth capacitor electrodes to establish electrical communication between said capacitor electrodes. The examiner notes that the conductive element (60) contacts the source drain region of the capacitor and therefore, electrically contacts the third and fourth capacitor electrodes.

In re claim 90, Prall et al. disclose the method wherein said second dielectric layer (56) is in contact with said first dielectric layer and with said third and fourth capacitor electrodes.

In re claim 91, Prall et al. disclose the method wherein said second and third portions of said first dielectric layer comprise an uppermost portion of said capacitors. The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole can be considered the uppermost portion (see Figure 8A and 18).

In re claim 92, Prall et al. disclose the method wherein said second and third portions of said first dielectric layer are spaced apart from respective said first and second capacitor electrodes (see Figure 8A and 18, horizontal surface of 44 is spaced apart from 42).

In re claim 93, Prall et al. disclose the method of forming capacitors, comprising:

forming first and second capacitor electrodes supported by a substrate, the first and second capacitors electrode comprising respective uppermost surfaces relative the substrate (42, 46); and

forming a dielectric layer (44) disposed between the first and second capacitor electrode, the dielectric layer comprising an uppermost surface relative the substrate, the uppermost surface of the dielectric layer being elevationally above one of the uppermost surface of the first and second capacitor electrodes and being coextensive with the other of the uppermost surfaces of the first and second capacitor electrodes; and

wherein the first and second capacitor electrodes and the dielectric layer form a single capacitor, and wherein the first and second capacitor electrodes are operatively isolated form adjacent capacitors (see Figure 11 or 20).

In re claim 94, Prall et al. disclose the method wherein at least one of the first and second capacitor electrodes is oriented substantially vertically relative the substrate (see Figure 8A or 18).

In re claim 95, Prall et al. disclose the method further comprising insulative material (36 or 45, see Figures 8A and 18, respectively) elevationally directly below and contacting the uppermost surface of the dielectric layer.

In re claim 96, Prall et al. disclose the method further comprising insulative material (56) elevationally directly above and contacting the uppermost surface of the dielectric layer.

In re claim 97, Prall et al. disclose the method further comprising a first insulative (36 or 45, see Figures 8A and 18) layer elevationally below and supporting the uppermost surface of the dielectric layer, and further comprising a second insulative layer (56) elevationally above and contacting the uppermost surface of the dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 78-87, and 98-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 5,866,453) in view of Sung (U.S. Patent No. 5,858,831).

In re claim 78, Prall et al. disclose the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (42) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate;

forming a dielectric layer (44) over said first capacitor electrode;

forming a second capacitor electrode (46) over one portion of said dielectric layer such that another portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 8A or Figure 18); and

forming a dielectric barrier (56) over said exposed portions of said dielectric layer.

Prall et al. do not disclose the method wherein the first capacitor electrode is formed of a roughened polysilicon. Sung discloses the method of forming the lower electrode of a roughened polysilicon (see column 7, lines 50-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first capacitor electrode of a roughened polysilicon in order to increase the surface area of the electrode, and thus increase the capacitance of the capacitor.

In re claim 79, Prall et al. discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 8A or Figure 18).

The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole can be considered the uppermost portion of the layer (as shown in Figures 8A or 18).

In re claim 80, Prall et al. discloses the method wherein the dielectric barrier (56) extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 10 and 19).

In re claim 81, Prall et al. discloses the method further comprising the steps of forming an opening (see Figure 10 and 19) in said dielectric barrier and forming a conductive element (60) extending into said opening to form an electrically conductive contact to said second capacitor electrode. The examiner notes that the conductive element (60) contacts the source drain region of the capacitor and therefore, electrically contacts the second capacitor electrode.

In re claim 82, Prall et al. disclose the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 9 and Figure 18).

In re claim 83, Prall et al. disclose the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 8A and Figure 18, horizontal surface of 44 is spaced apart from 42).

In re claim 84, Prall et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 8A and 18, horizontal surface of 44 is spaced apart from 42).

In re claim 85, Prall et al. disclose the method further comprising insulative material (36 or 45 as seen in Figures 8A and 18, respectively) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, Prall et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein the one portion of the said dielectric layer contacts said first capacitor electrode (see Figure 8A and 18, horizontal surface of 44 is spaced apart from 42).

In re claim 87, Prall et al. disclose the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (see Figure 8A and Figure 18).

In re claim 98, Sung discloses the method wherein the roughened polysilicon comprises hemispherical grain polysilicon (see column 7, lines 50-55).

In re claim 99, Sung discloses the method wherein the roughened polysilicon is hemispherical grain polysilicon but does not disclose the method of utilizing cylindrical grain polysilicon. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a cylindrical grained silicon rather than a hemispherical grain silicon. The method of forming cylindrical grain silicon is well known and used in

the art and can be interchangeable with hemispherical grain silicon in the art. Both grained silicon specie allow increase the surface area of a capacitor electrode, and thus increasing the capacitance of the formed capacitor. Further the examiner notes that it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Claims 78-87 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 5,866,453) in view of Parekh et al. (U.S. Patent No. 5,918,122).

In re claim 78, Prall et al. disclose the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (42) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate;

forming a dielectric layer (44) over said first capacitor electrode;

forming a second capacitor electrode (46) over one portion of said dielectric layer such that another portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 8A or Figure 18); and

forming a dielectric barrier (56) over said exposed portions of said dielectric layer.

Prall et al. do not disclose the method wherein the first capacitor electrode is formed of a roughened polysilicon. Parekh et al. disclose the method of forming the lower electrode of a roughened polysilicon (see column 6, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first capacitor electrode of a roughened polysilicon in order to increase the surface area of the electrode, and thus increase the capacitance of the capacitor.

In re claim 79, Prall et al. discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 8A or Figure 18).

The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole can be considered the uppermost portion of the layer (as shown in Figures 8A or 18).

In re claim 80, Prall et al. discloses the method wherein the dielectric barrier (56) extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 10 and 19).

In re claim 81, Prall et al. discloses the method further comprising the steps of forming an opening (see Figure 10 and 19) in said dielectric barrier and forming a conductive element (60) extending into said opening to form an electrically conductive contact to said second capacitor electrode. The examiner notes that the conductive element (60) contacts the source drain region of the capacitor and therefore, electrically contacts the second capacitor electrode.

In re claim 82, Prall et al. disclose the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 9 and Figure 18).

In re claim 83, Prall et al. disclose the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 8A and Figure 18, horizontal surface of 44 is spaced apart from 42).

In re claim 84, Prall et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 8A and 18, horizontal surface of 44 is spaced apart from 42).

In re claim 85, Prall et al. disclose the method further comprising insulative material (36 or 45 as seen in Figures 8A and 18, respectively) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, Prall et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein the one portion of the said dielectric layer contacts said first capacitor electrode (see Figure 8A and 18, horizontal surface of 44 is spaced apart from 42).

In re claim 87, Prall et al. disclose the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (see Figure 8A and Figure 18).

In re claim 99, Parekh et al. disclose the method wherein the roughened polysilicon comprises cylindrical grain polysilicon.

Claims 78-87 and 98-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent Appl. 2001/0044181) in view of Sung (U.S. Patent No. 5,858,831).

In re claim 78, Nakamura discloses the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (46) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate (see Figure 3C);

forming a dielectric layer (52) over said first capacitor electrode;

forming a second capacitor electrode (56) over a portion of said dielectric layer such that an other portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 4A); and

forming a dielectric barrier (64, see Figure 5A) over said exposed portions of said dielectric layer.

Nakamura does not disclose the method wherein the first capacitor electrode is formed of a roughened polysilicon. Sung discloses the method of forming the lower electrode of a roughened polysilicon (see column 7, lines 50-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first capacitor electrode of Nakamura with a roughened polysilicon in order to increase the surface area of the electrode, and thus increase the capacitance of the capacitor.

In re claim 79, Nakamura discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 4A).

In re claim 80, Nakamura discloses the method wherein the dielectric barrier extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 5A).

In re claim 81, Nakamura discloses the method further comprising the steps of forming an opening in said dielectric barrier and forming a conductive element (60) extending into said opening to form an electrically conductive contact to said second capacitor electrode (see Figure 5B).

In re claim 82, Nakamura discloses the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 4A).

In re claim 83, Nakamura discloses the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 4A, extends vertically away and apart from first capacitor electrode).

In re claim 84, Nakamura discloses the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 85, Nakamura discloses the method further comprising insulative material (58) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, Nakamura discloses the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein said dielectric layer comprises other portions contacting said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 87, Nakumura discloses the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (see Figure 4A).

In re claim 98, Sung discloses the method wherein the roughened polysilicon comprises hemispherical grain polysilicon (see column 7, lines 50-55).

In re claim 99, Sung discloses the method wherein the roughened polysilicon is hemispherical grain polysilicon but does not disclose the method of utilizing cylindrical grain polysilicon. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a cylindrical grained silicon rather than a hemispherical grain silicon. The method of forming cylindrical grain silicon is well known and used in the art and can be interchangeable with hemispherical grain silicon in the art. Both grained silicon specie allow increase the surface area of a capacitor electrode, and thus increasing the capacitance of the formed capacitor. Further the examiner notes that it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll

Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Claims 78-87 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent Appl. 2001/0044181) in view of Parekh et al. (U.S. Patent No. 5,918,122).

In re claim 78, Nakamura discloses the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (46) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate (see Figure 3C);

forming a dielectric layer (52) over said first capacitor electrode;

forming a second capacitor electrode (56) over a portion of said dielectric layer such that an other portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 4A); and

forming a dielectric barrier (64, see Figure 5A) over said exposed portions of said dielectric layer.

Nakamura does not disclose the method wherein the first capacitor electrode is formed of a roughened polysilicon. Parekh et al. disclose the method of forming the lower electrode of a roughened polysilicon (see column 6, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first capacitor electrode of Nakamura with a roughened polysilicon in order to

increase the surface area of the electrode, and thus increase the capacitance of the capacitor.

In re claim 79, Nakamura discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 4A).

In re claim 80, Nakamura discloses the method wherein the dielectric barrier extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 5A).

In re claim 81, Nakamura discloses the method further comprising the steps of forming an opening in said dielectric barrier and forming a conductive element (60) extending into said opening to form an electrically conductive contact to said second capacitor electrode (see Figure 5B).

In re claim 82, Nakamura discloses the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 4A).

In re claim 83, Nakamura discloses the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 4A, extends vertically away and apart from first capacitor electrode).

In re claim 84, Nakamura discloses the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 85, Nakamura discloses the method further comprising insulative material (58) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, Nakamura discloses the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein said dielectric layer comprises other portions contacting said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 87, Nakumura discloses the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (see Figure 4A).

In re claim 99, Parekh et al. disclose the method wherein the roughened polysilicon comprises cylindrical grain polysilicon.

Response to Arguments

Applicant's arguments with respect to claims 78-97 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claim 100 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the limitations of a method of forming a bit line elevationally below the first, second third and fourth capacitor electrodes and elevationally below the first and second dielectric layers in combination with together limitations of independent claim 88. Prall clearly discloses a capacitor under bit line structure in which the bit line is formed above the capacitor structures.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk